DELAY ANALYSIS SYSTEM

FIELD OF THE INVENTION

5   The present invention relates to a system for analyzing a delay in a logic circuit device, and more particularly to a library for delay analysis.

BACKGROUND OF THE INVENTION

When calculating a delay in a logic circuit in a
10   conventional delay simulation system, a delay analysis library containing circuit connection information and delay information on the basic elements (such as AND elements) of the circuit is used.

The conventional delay analysis library contains
15   connection information as well as delay information which is composed of the delay time of each rise and fall.   But, it does not contain logic information on the circuit.

For this reason, the circuit delay analysis uses the worst delay times stored in the delay analysis library,
20   sometimes preventing the delay analysis from being made correctly.

An earlier patent disclosure dealing with delay analysis is found, for example, in Japanese Patent Kokai Publication JP-A No. Hei 1-271869(1989).   In   that
25   publication, a propagation delay time calculation method

for use in calculating propagation delay times is proposed. In this method, the calculation is made by calculating the load and wiring capacity of the output terminals and the rise time and fall time of each gate.

5   SUMMARY OF THE DISCLOSURE

During the eager investigation toward the present invention, following problems have been encountered.

As described above, the conventional delay analysis library, in which no logic value table is stored, contains

10   information on the worst delay times for use in delay time analysis.   As shown in FIG. 7, the calculation with the use of such a library results in the total delay time of 28ns being assumed for the signal flowing through terminal 2 (The delay time between input terminal 2 and the output terminal

15   3 is 8ns..).   (As will be described later, the actual delay time is 24ns.)

In view of the foregoing, it is an object of the present invention to provide a delay analysis system and a delay analysis method for analyzing delays and calculating

20   delay times considering circuit logic information.

To achieve the above object, the delay analysis library in accordance with the present invention contains not only connection information on a plurality of circuits and delay time information on the rises and falls of the

25   input and output terminals but also logic information on the

logic operation of said plurality of circuits.

When making the delay analysis of a logic circuit, the system in accordance with the present invention selects a delay time information according to the logic operation

5 of the circuits included in the logic circuit, the delay time being between the input terminals and output terminals of the circuits, from the library which contains the delay time information on the rises and falls of the input terminals and output terminals.

10 BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows the diagrams illustrating a delay analysis library used in an embodiment of the present invention. FIG. 1(a) shows circuit connection information, FIG. 1(b) shows delay time information on the rise and fall

15 of the input terminals and output terminals, and FIG. 1(c) shows logic information (truth table).

FIG. 2 is a diagram showing the embodiment of the present invention. The figure shows an example of a logic circuit.

20 FIG. 3 is a diagram illustrating the embodiment of the present invention. The figure is a waveform diagram showing the rise and fall delay patterns of a 2-input AND circuit.

FIG. 4 is a diagram showing the embodiment of the

25 present invention.

FIG. 5 is a diagram showing the embodiment of the present invention.

FIG. 6 is a diagram showing the embodiment of the present invention. It shows the delay analysis result of

5 the logic circuit shown in FIG. 2.

FIG. 7 is a diagram showing the embodiment of the present invention. It shows the delay analysis result of the logic circuit shown in FIG. 2.

DESCRIPTION OF PREFERRED EMBODIMENT

10 An embodiment of the present invention will now be described more in detail. In a system where a delay analysis library is used in which circuit connection information on the basic circuits such as combinational circuits composed of AND elements, OR elements, NAND

15 elements, and NOR elements and other sequential circuits and delay time information on the rises and falls of the input and output terminals of the basic circuits are stored, the preferred embodiment of the present invention also contains, in the library, logical operation information which

20 represents a correspondence between the logical values of each input terminal and their output logical values of the basic circuit.

When making the delay analysis of a logic circuit, the delay analysis system according to the present invention

25 selects, for each basic circuit of the logic circuit, the

delay time between an input terminal and an output terminal from the delay time information on the rises and falls of the input and output terminals of the basic circuit, stored in the library, according to the logical operation of the

5 basic circuit specified by the logical operation information. The system uses the delay time of the basic circuit, which is obtained in this manner, in calculating the delay time of the logical circuit.

The delay analysis system according to the present

10 invention, which references the library to select the delay time of a circuit logical operation and calculates the delay of a logic circuit using the selected delay time, may be implemented by a computer-executable program.

Thus, in the embodiment according to the present

15 invention, delay analysis considering the truth table may be made to calculate more accurate delay times.

EXAMPLE

An embodiment of this invention will now be described more in detail with reference to the drawings.

20 FIG. 1 illustrates an embodiment of the present invention. In the following description, the library for a 2-input AND element, such as the one shown in FIG. 1(a), is used as the basic gate circuit.

The library contains information on circuit

25 connections and on the delay time for each rise/fall

combination.　That is, it contains information on the delay
time of each combination of input pins 1 and 2 (terminals
1 and 2) and output pin 3(terminal 3).

The table shown in FIG. 1(b) represents delay times
for the combinations of an input pin and an output pin as
they rise or fall.　For example, on the first line, the
delay time of 1 ns means that the delay between the time the
signal at the input pin (terminal 1) of a 2-input AND element
goes from low to high (rises) and the time the signal at the
output pin (terminal 3) goes from low to high (rises) is 1
ns.　Similarly, on the fifth line, the delay time of 2 ns
means that the delay between the time the signal at the input
pin (terminal 1) of a 2-input AND element goes from low to
high (rises) and the time the signal at the output pin
(terminal 3) goes from low to high (falls) is 5 ns.　Note
that delay time information on the rise and fall of input
and output pins, such as that shown in FIG. 1(b), is
contained also in the conventional delay analysis library.

An embodiment according to the present invention
uses a truth table (table showing the correspondence between
input logical values and output logical values) such as the
one shown in FIG. 1(c).

Consider the logic circuit composed of the 2-input
AND circuit shown in the library in FIG. 1 and its peripheral
circuits.

The operation of the 2-input AND circuit is as shown in the truth table in FIG. 1 (c). The operation is shown also in FIG. 3 using the timing waveforms and the inputs having change points to be considered when calculating the

5 delay time.

The inputs to be selected and their rises/falls are selected from those shown in FIG. 3 for each of the rise and the fall of the output signal at the output pin (terminal 3). The result is shown in FIG. 4.

10 That is, FIG. 3 indicates that the output (terminal 3) rises when both inputs 1 and 2 (terminals 1 and 2) of the 2-input AND element rise. At that time, the output rises when one of the inputs which rises later rises. That is, for the 2-input AND element, the delay between the time input

15 1 (terminal 1) rises and the time the output (terminal 3) rises is 1 ns, and the delay between the time input 2 (terminal 2) rises and the time the output (terminal 3) rises is 5 ns. When both input 1 and input 2 rise, the output (terminal 3) rises when terminal 2 rises. Thus, when

20 making a delay analysis, terminal 2 with the delay time of 5 ns is selected as the terminal which rises later.

When inputs 1 and 2 (terminals 1 and 2) of the 2-input AND element fall, the output (terminal 3) fall. At that time, the output falls when one of the inputs which falls

25 earlier falls. That is, when input 1 (terminal 1) falls,

the delay time of the output (terminal 3) is 4 ns; when input
2 (terminal 2) falls, the delay time of the output (terminal
3) is 8 ns.   Thus, when making a delay analysis, terminal
1 with the delay time of 4 ns is selected as the terminal

5 which falls earlier. When inputs 1 and 2 are rise/fall, no
terminal is selected for delay analysis.

From the combinations of inputs shown in FIG. 1(b),
those inputs which both rise or fall are selected.   They
are enclosed by boxes in FIG. 5.

10 Next, the calculation of the maximum delay time
between the input and the output of the whole circuit through
the analysis of the logic circuit shown in FIG. 2 is
described.   This requires the tracing of the circuit.   In
this embodiment,   the DFS (Depth First Search) used in the

15 graph theory is used as the trace technology.

The following describes the calculation of the
maximum delay time in two cases: one is the case when the
signal at the output terminal (terminal 3) of the 2-input
AND circuit rises and the other is the case when it falls.

20 First, when the signal at the output terminal
(terminal 3) rises, the flow of the signal through terminal
2 which rises later (delay time of 5 ns) is used based on
the description in FIGS. 4 and 5.   As a result, the total
delay time (worst value) from the input to the output of the

25 circuit is calculated at 25 ns (10 ns + 5 ns + 10 ns) as shown

in FIG. 6.

On the other hand, when the signal at the output terminal (terminal 3) falls, the flow of the signal through terminal 1 which falls earlier (delay time of 4 ns) is used

5   based on the description in FIGS. 4 and 5. As a result, the total delay time (worst value) is calculated at 24 ns (10 ns + 4 ns + 10 ns) as shown in FIG. 7.

The present invention also applies when calculating the minimum delay time.

10   As described above, the embodiment according to the present invention uses the truth table when making a delay analysis with the use of a delay analysis library, thereby giving more accurate delay times.

It should be noted that other objects of the present

15   invention will become apparent in the entire disclosure and that modifications may be done without departing the gist and scope of the present invention as disclosed herein and appended herewith.

Also it should be noted that any combination of the

20   disclosed and/or claimed elements, matters and/or items may fall under the modifications aforementioned.